IN THE CLAIMS

1-36 (canceled)

37. (Currently Amended) A content addressable memory (CAM) apparatus comprising:

an array of CAM cells to store data to be compared with a comparand value;

a select circuit to store a plurality of segment-select values, each segment-select value indicating which of a plurality of segments of input data is to source a respective bit of the comparand value; ~~and~~

a filter circuit to store filter data that indicates, within each of the plurality of segments indicated by the segment select values, selected bits, if any, to be included within the comparand value; and

switch circuitry to output, as the comparand value, ~~one or more~~ the selected bits of each of the plurality of segments of input data ~~indicated by the select circuit to be a source of a bit of the comparand value~~.

38. (Previously added) The CAM apparatus of claim 37 wherein the select circuit comprises:

a plurality of memory storage circuits to store the plurality of segment-select values; and

a plurality of compare circuits to compare the plurality of segment-select values with input segment information to generate a plurality of select signals.

39. (Previously added) The CAM apparatus of claim 38 wherein the plurality of compare circuits and the plurality of memory storage circuits form a plurality of CAM cells.

40. (Previously added) The CAM apparatus of claim 38 wherein the switch circuitry

comprises L rows of programmable switch circuits coupled to receive L input bits of the input data and coupled to receive the select signals from the select circuit.

41. (Previously added) The CAM apparatus of claim 40 wherein the L inputs bits are one of N segments of M input bits where M is equal to N multiplied by L.

42. (Previously added) The CAM apparatus of claim 37 wherein the switch circuitry comprises a plurality of programmable switch elements, and wherein the CAM apparatus further comprises a program circuit coupled to the switch circuitry to program the plurality of programmable switch elements.

43. (Previously added) The CAM apparatus of claim 37 wherein the switch circuitry comprises a cross-bar switch.

44. (Previously added) The CAM apparatus of claim 37 further comprising a comparand register coupled between the switch circuitry and the array of CAM cells, the comparand register to store the comparand value output from the switch circuitry.

45. (Previously added) The CAM apparatus of claim 44 further comprising a global mask register coupled between the comparand storage register and the array of CAM cells.

46. (Previously added) The CAM apparatus of claim 37 wherein at least one bit of the input data has a first bit position in the input data and a second, different bit position in the comparand value.

47. (Previously added) The (CAM) apparatus of claim 37 wherein the array of CAM cells

comprises a plurality of CAM array blocks each having a plurality of rows of CAM cells.

48. (Previously added) The CAM device of claim 47 wherein the switch circuitry is coupled to provide the comparand value to each of the plurality of CAM array blocks.

49. (Previously added) The CAM apparatus of claim 47 wherein the select circuit and the switch circuitry correspond to a first CAM array block of the plurality of CAM array blocks, and wherein the CAM apparatus further comprises at least one additional select circuit and at least one additional switch circuitry that correspond to a second CAM array block of the plurality of CAM array blocks.

50. (Previously added) The CAM apparatus of claim 37 wherein the array of CAM cells are disposed in rows and columns, with the rows being segmented to form a plurality of columns of row segments, each row segment including a plurality of CAM cells.

51. (Previously Submitted) The CAM apparatus of claim 50 wherein the select circuit and the switch circuitry correspond to a first column of the plurality of columns of row segments, and wherein the CAM apparatus further comprises at least one additional select circuit and at least one additional switch circuitry that correspond to a second column of the plurality of columns of row segments.

52. (Previously added) The CAM apparatus of claim 50, wherein the number of CAM cells included in each row segment matches a width of the comparand value, and wherein the switch circuitry is coupled to provide the comparand value to each of the plurality of columns of row segments.

53. (Currently Amended) A content addressable memory (CAM) apparatus comprising:

an array of CAM cells to store data to be compared with a comparand value;

means for storing a plurality of segment-select values, each segment-select value indicating which of a plurality of segments of input data is to source a respective bit of the comparand value; ~~and~~

means for storing filter data that indicates, within each of the plurality of segments indicated by the segment select values, selected bits, if any, to be included within the comparand value; and

means for outputting, as the comparand value, one or more bits of each of the plurality of segments of input data indicated by the select circuit to be a source of a bit of the comparand value.

54. (Previously added) The CAM apparatus of claim 53, wherein the means for outputting comprises a cross-bar switch.

55. (Currently Amended) A method of operation within a content addressable memory device, the method comprising:

storing a plurality of segment-select values, each segment-select value indicating which of a plurality of segments of input data is to source a respective bit of a comparand value;

storing filter data for indicating, within each of the plurality of segments indicated by the segment select values, selected bits, if any, to be included within the comparand value;

outputting, as a comparand value, one or more bits of each of the plurality of segments of input data indicated by the segment-select values to be a source of a bit of the

comparand value; and

comparing the comparand value to contents of an array of CAM cells.

56. (Currently Amended) A method comprising:

receiving a plurality of segments of input data in a content addressable memory (CAM) apparatus having an array of CAM cells;

storing a plurality of segment-select values within the CAM apparatus, each segment-select value indicating which of the plurality of segments of input data is to source a respective bit of the comparand value; ~~and~~

storing filter data that indicates, within each of the plurality of segments indicated by the segment select values, selected bits, if any, to be included within the comparand value; and

selectively enabling, in response to the plurality of segment-select values, programmed switch circuitry to filter at least one bit of the input data to generate at least one comparand bit for the array of CAM cells.

57. (Previously added) The method of claim 56 wherein selectively enabling programmed switch circuitry to filter at least one bit of the input data comprises selectively enabling at least one programmed switch circuit to couple one bit of the input data to at least one bit position of a comparand storage element.

58. (Previously added) The method of claim 56 further comprising comparing the comparand bit with data stored in the array of CAM cells.

59. (New) The content addressable memory of claim 37 wherein the switch circuit comprises a cross-bar switch having a plurality of switching junctions, wherein each switching junction comprises at least first and second transistors disposed in series, wherein the first transistor is configured to be gated by a bit-value stored within the filter circuit, and the second transistor is configured to be gated by a signal produced by the select circuit.